

STM32MP13XXAE_LPDDR3

Schematics not complete, only for layout example

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STM32MP13XXAE_LPDDR3_TOP.SchDoc



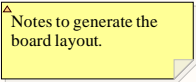
Note

Legend

General comment such as function title, configuration, ...

Text to be added to silkscreen.

Warning text.



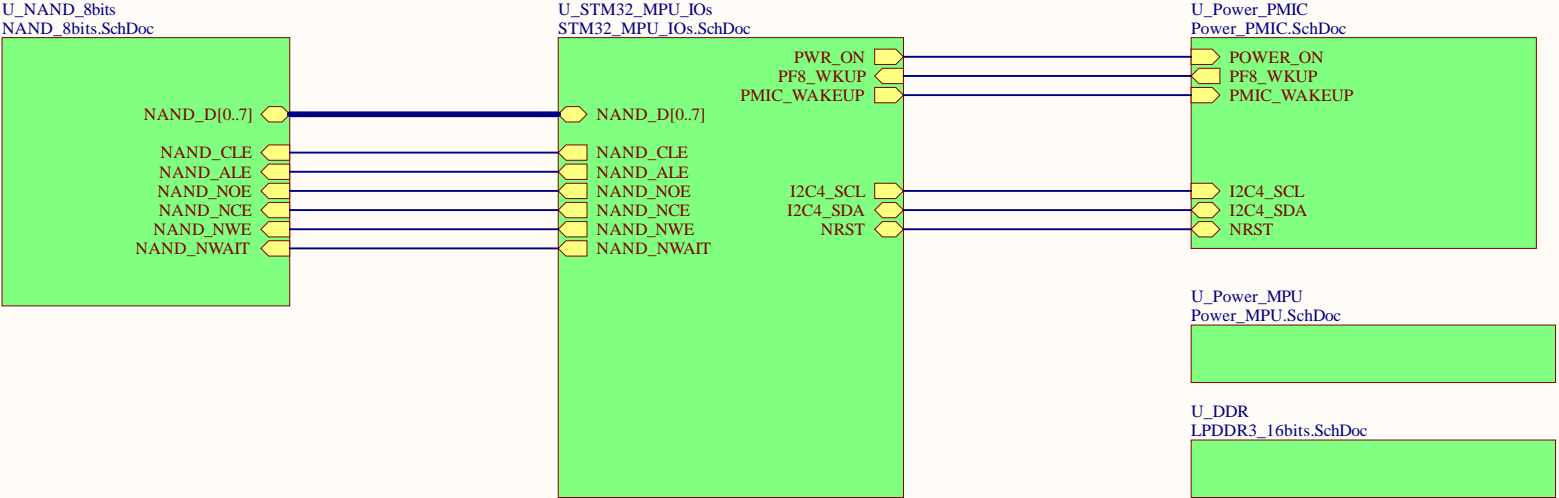
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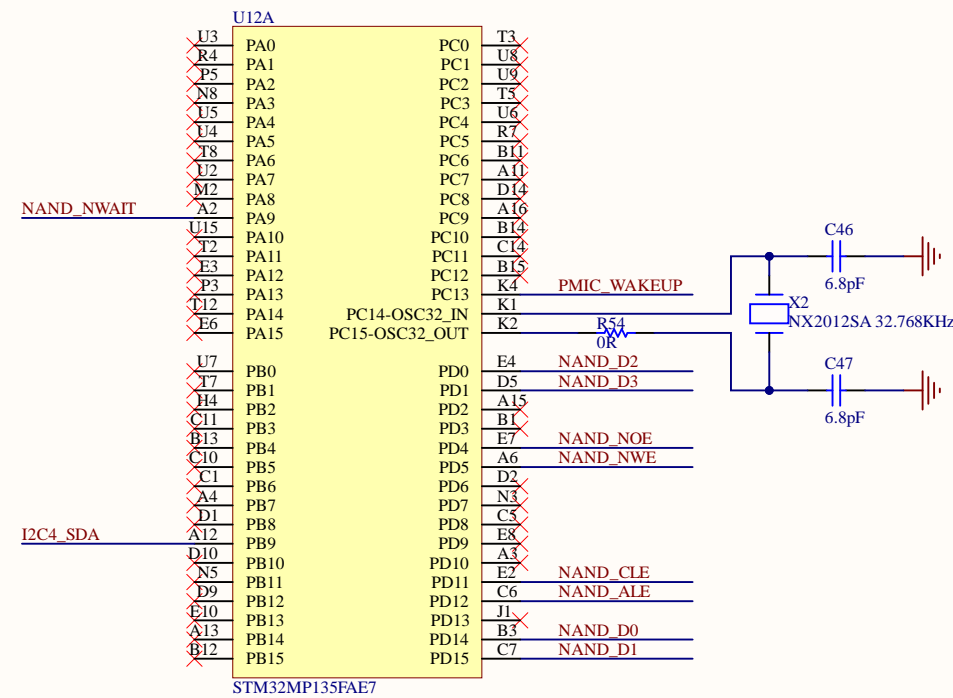
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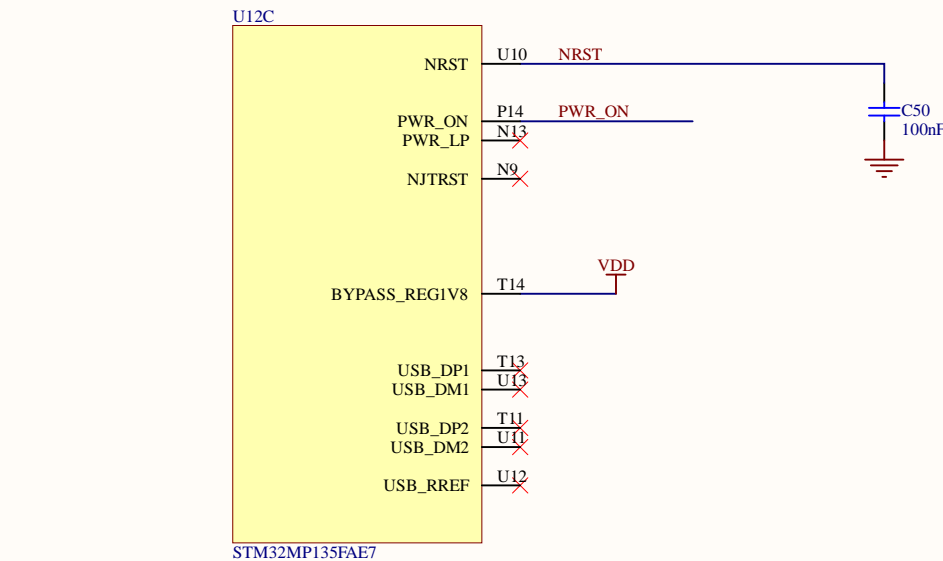
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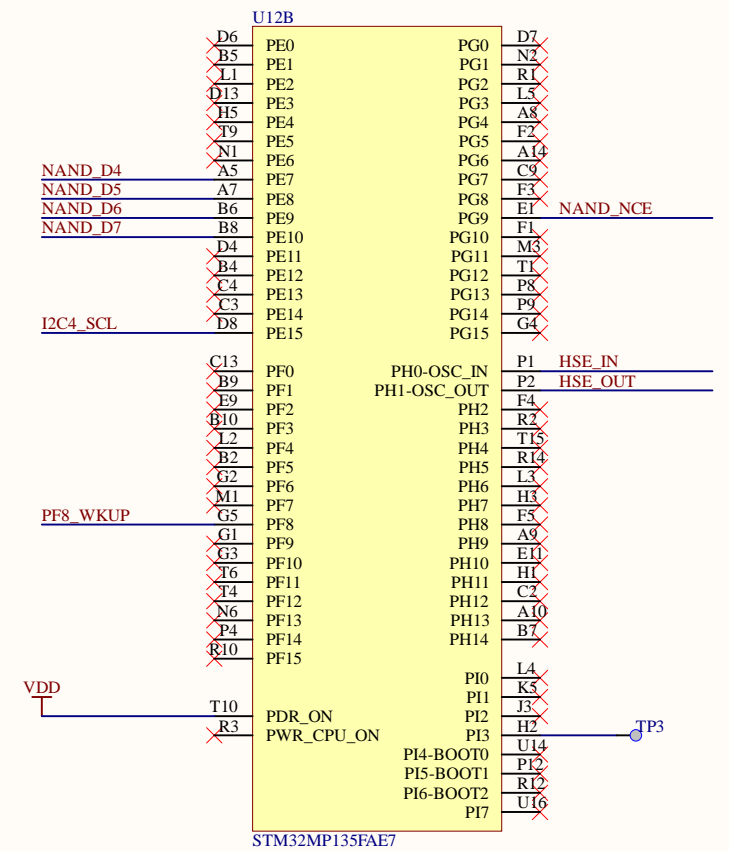




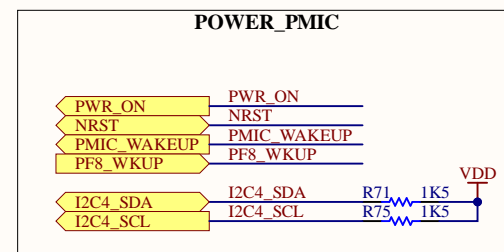
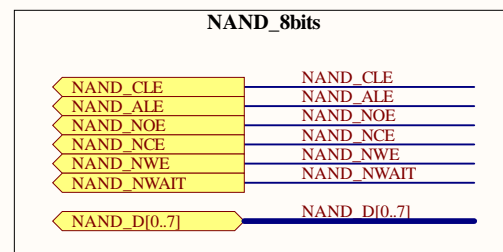
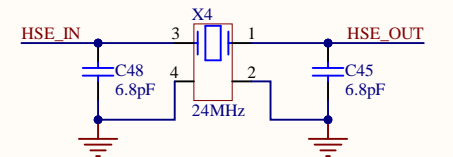
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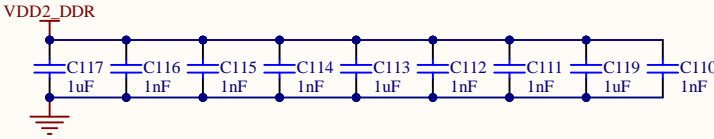
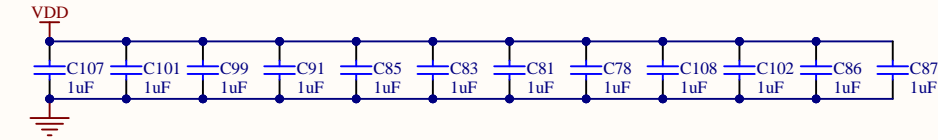
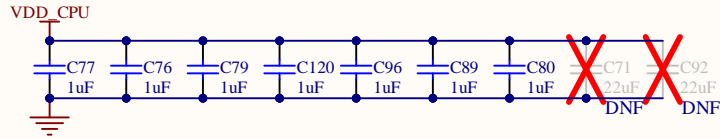
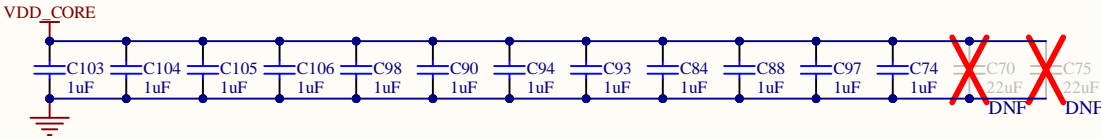


STM32MP135FAE7

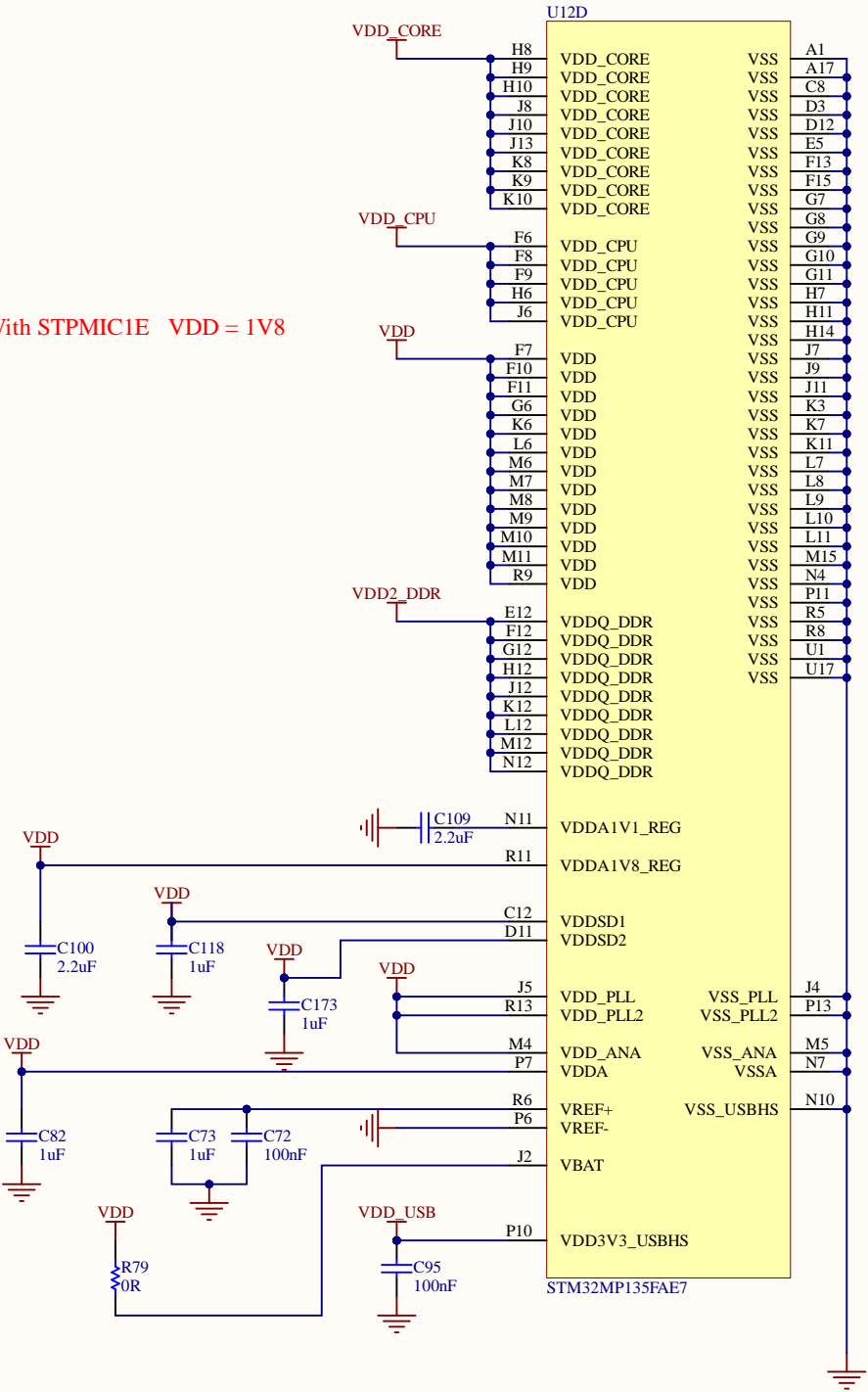


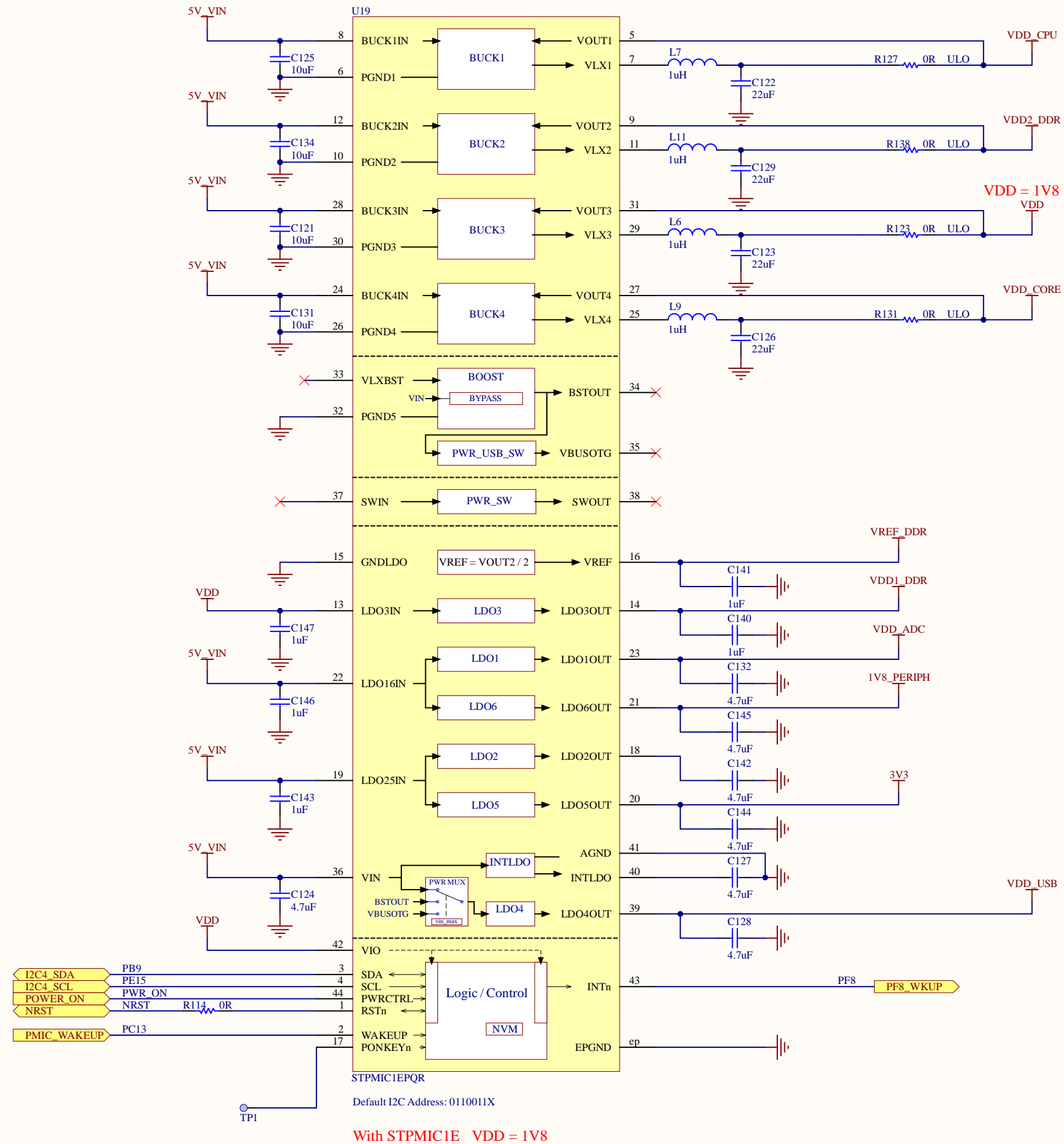
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With STPMIC1E VDD = 1V8





With STPMIC1E VDD = 1V8

